

**Rugged RF & Optical Solutions Over OpenVPX
Prepare Mil/Aero Customers For the Next Generation
of System Performance**

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SPECIAL FEATURES

14 **Rugged RF & Optical Solutions Over OpenVPX Prepare Mil/Aero Customers For the Next Generation of System Performance**

By Gary Stein (Principal Engineer) and Jake Braegelmann (VP of Business Development), New Wave Design & Verification

COTS COMPANY PROFILE:

20 **Leidos**

By John Reardon, COTS Journal

COT'S PICKS

24 **Editor's Choice for January**

Cover Image

A U.S. Marine with Special Purpose Marine Air-Ground Task Force-Crisis Response-Africa 20.1, Marine Forces Europe and Africa, searches for targets to engage with Spanish Marines with 1st Landing Battalion, and Spanish Army soldiers with Airborne Brigade VI during Exercise Trueno in Chinchilla, Spain, Dec. 18.



DEPARTMENTS

6

The Inside Track



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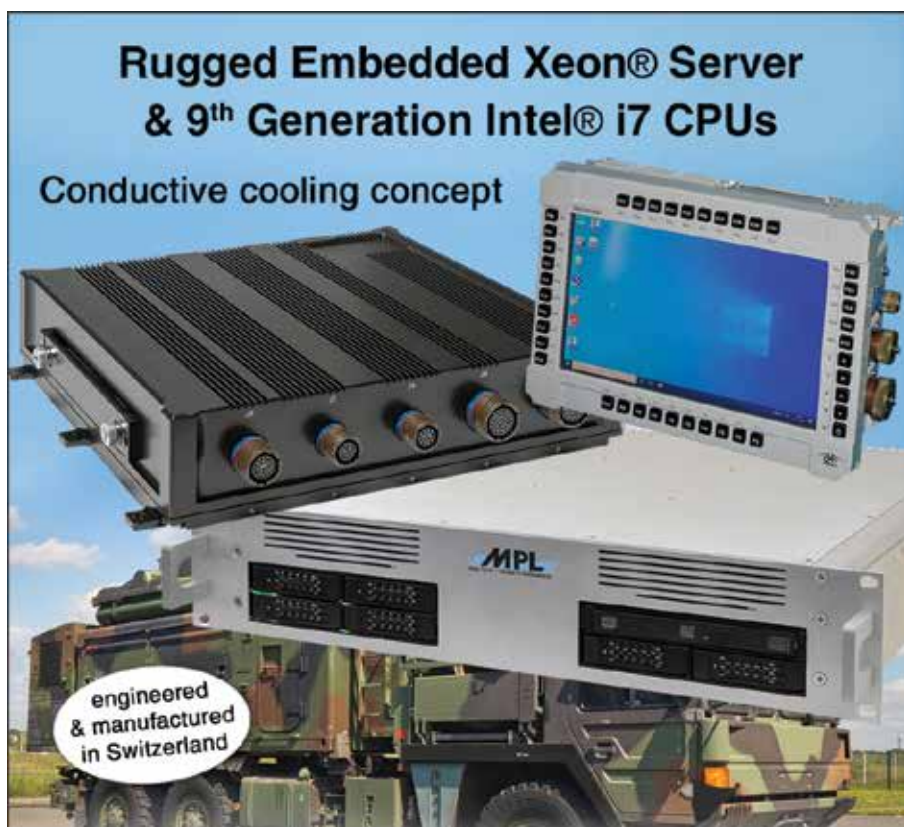
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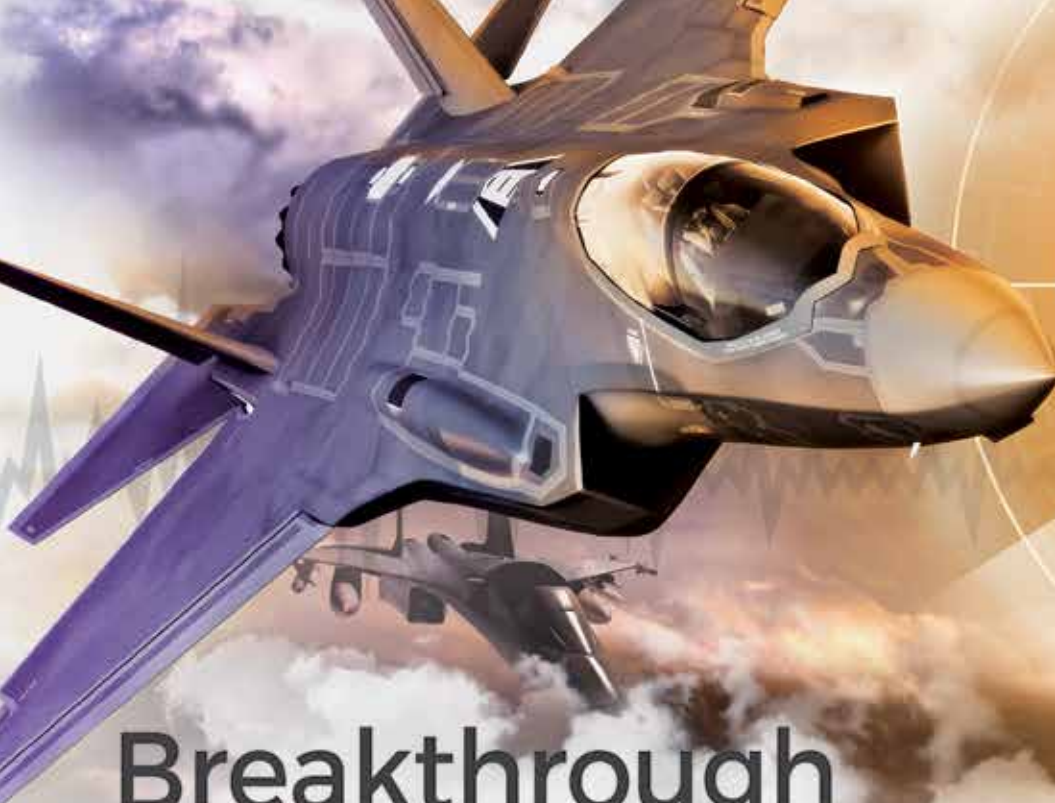
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The **INSIDE TRACK**

Lockheed Martin delivered the 134th F-35 aircraft in 2019, exceeding the joint government and industry delivery goal of 131 aircraft.

One hundred and thirty-four deliveries represent a 47% increase from 2018 and nearly a 200 percent production increase from 2016. Next year, Lockheed Martin plans to deliver 141 F-35s and is prepared to increase production volume year-over-year to hit peak production in 2023.

Lockheed Martin BF-91

"This achievement is a testament to the readiness of the full F-35 enterprise to ramp to full-rate production and we continue to focus on improving on-time deliveries across the entire weapons system," said Greg Ulmer, Lockheed Martin vice president and general manager of the F-35 program. "We have met our annual delivery targets three years in a row and continue to increase production rates, improve efficiencies and reduce costs. The F-35 is the most capable fighter jet in the world, and we're now delivering the 5th Generation weapon system at a cost equal to or lower than a less capable 4th Generation legacy aircraft."

The 134th aircraft is a Short Takeoff and Vertical Landing (STOVL) model for the United

States Marine Corps. In 2019, deliveries included 81 F-35s for the United States, 30 for international partner nations and 23 for Foreign Military Sales customers.

Unit and Sustainment Costs Decrease, Readiness Improving

Using lessons learned, process efficiencies, production automation, facility and tooling upgrades, supply chain initiatives and more – the F-35 enterprise continues to significantly improve efficiency and reduce costs.

The price of an F-35A is now \$77.9 million, meeting the \$80 million goal a year earlier than planned.

The F-35's mission readiness and sustainment costs continue to improve with the global fleet averaging greater than 65% mission capable rates, and operational squadrons consistently performing near 75%.

Lockheed Martin's sustainment cost per aircraft per year has also decreased four con-

secutive years, and more than 35% since 2015.

Program Maturity and Economic Impact

With more than 490 aircraft operating from 21 bases around the globe, the F-35 plays a critical role in today's global security environment.

Today, 975 pilots and 8,585 maintainers are trained, and the F-35 fleet has surpassed more than 240,000 cumulative flight hours. Eight nations have F-35s operating from a base on their home soil, eight services have declared Initial Operating Capability and four services have employed F-35s in combat operations.

In addition to strengthening global security and partnerships, the F-35 provides economic stability to the U.S. and international partners by creating jobs, commerce and security, and contributing to the global trade balance. Thousands of men and women in the U.S. and around the world build the F-35. With more than 1,400 suppliers in 47 states and Puerto Rico, the F-35 Program supports more than 220,000 jobs.



The INSIDE TRACK

General Atomics Announces NASA Deep Space Atomic Clock in Nominal Operation

General Atomics Electromagnetic Systems (GA-EMS) announced that in early November NASA ended the commissioning phase of the Deep Space Atomic Clock (DSAC), the primary payload on-board GA-EMS' Orbital Test Bed (OTB) satellite, with DSAC now in nominal operation to demonstrate its capabilities supporting deep space navigation and exploration. OTB was launched from Cape Canaveral on June 25, 2019 on a SpaceX Falcon Heavy rocket.

"OTB continues to operate nominally, and we are excited that DSAC is performing as anticipated," stated Scott Forney, president of GA-EMS. "We continue to provide operation services to the Jet Propulsion Laboratory (JPL) and NASA for the currently scheduled year-long trial of DSAC's functionality and utility for one-way-based space navigation. We are very excited to be supporting a project that has the potential to change the future of deep space navigation."

DSAC is a miniaturized, ultra-precise, mercury-ion atomic clock designed and built at NASA's JPL for NASA Space Technology Mission Directorate's Technology Demonstration Missions

Program. DSAC provides extreme accuracy and greater stability than today's best navigation clocks to support exploration deeper into the solar system, as well as potentially provide benefits to Earth users worldwide.

"In addition to DSAC, commissioning of the other demonstration payloads on-board OTB continues according to each customer's schedule," stated Nick Bucci, vice president of Missile Defense and Space Systems at GA-EMS. "We anticipate OTB to remain mission capable for up to seven years, providing customers with a significant timeframe to perform and complete their individual mission objectives."

GA-EMS' OTB is a configurable, versatile platform designed to space-qualify multiple payloads on a single satellite. OTB increases the number of flight opportunities for customers looking to launch their payload into orbit without bearing the costly burden of designing, building and launching a dedicated spacecraft. GA-EMS works closely with customers to design and build OTB satellites that simultaneously meet multiple customer mission objectives and requirements. Launch and mission operation services are also provided by GA-EMS to support the full mission lifecycle for each customer payload.



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The **INSIDE TRACK**

SRC Awarded Blanket Purchase Agreement to Provide U.S. Air Force with Intelligence Mission Data Support Services

SRC, Inc., has been awarded a General Services Administration blanket purchase agreement to provide intelligence mission (IMD) support services to the U.S. Air Force's National Air and Space Intelligence Center (NASIC). The agreement has a \$376 million ceiling over five base years and five additional option years, starting October 1, 2019.

SRC, Inc., has been awarded a General Services Administration blanket purchase agreement to provide intelligence mission (IMD) support services to the U.S. Air Force. NASIC's IMD program supports Wright-Patterson Air Force Base in performing IMD staging, engineering analysis, technologies development and training activities.

"We are proud to be able to provide the highly specialized intelligence mission data engineering services and tools that the Air Force relies on," said Paul G. Tremont, CEO of SRC, Inc.

"We look forward to working with our industry partners to help ensure that our warfighters can complete their missions and return home safely."

SRC, Inc. was named one of the two contractor teaming arrangement awardees. As a team lead, SRC will work with teammates that include Altamira, Booz Allen Hamilton, Dynetics and Macauley-Brown. Work is expected to be performed across SRC's offices in Dayton, OH; Syracuse, NY; Charlottesville, VA; and San Antonio, TX.



NXP Completes Acquisition of Marvell's Wi-Fi and Bluetooth Connectivity Assets

NXP Semiconductors N.V. announced the completion of the acquisition of the wireless connectivity assets from Marvell (NASDAQ: MRVL), pursuant to the terms of the previously announced agreement from May 2019.

About NXP Semiconductors

NXP Semiconductors N.V. (NASDAQ: NXPI) enables secure connections for a smarter world, advancing solutions that make lives easier, better, and safer. As the world leader in secure connectivity solutions for embedded applications, NXP is driving innovation in the automotive, industrial & IOT, mobile, and communication infrastructure markets. Built on more than 60 years of com-

bined experience and expertise, the company has approximately 30,000 employees in more than 30 countries and posted revenue of \$9.41 billion in 2018.



The INSIDE TRACK

2019 ACM Gordon Bell Prize Awarded to ETH Zurich Team for Developing Simulation that Maps Heat in Transistors

DaCe OMEN Framework Could Help Industry Design Better and More Efficient Computer Chips

ACM, the Association for Computing Machinery, named a six-member team from the Swiss Federal Institute of Technology (ETH) Zurich recipients of the 2019 ACM Gordon Bell Prize for their project, “A Data-Centric Approach to Extreme-Scale Ab initio Dissipative Quantum Transport Simulations.”

The ETH Zurich team introduced DaCe OMEN, a new framework for simulating the transport of electrical signals through nanoscale materials (such as the silicon atoms used in transistors). To better understand the thermal properties of transistors, the team simulated how electricity would be transported through a two-dimensional slice of a transistor consisting of 10,000 atoms. The ETH Zurich researchers simulated the 10,000-atom system 14 times faster than an earlier framework that was used for a 1,000-atom system. The DaCe OMEN code they developed for the simulation has been run on two top-6 hybrid supercomputers, reaching a sustained performance of 85.45 Pflop/s on 4,560 nodes of Summit (42.55% of the peak) in double precision, and 90.89 Pflop/s in mixed precision.

The ACM Gordon Bell Prize tracks the progress of parallel computing and rewards innovation in applying high performance computing to challenges in science, engineering, and large-scale data analytics. The award was presented by ACM President Cherri Pancake and Arndt Bode, Chair of the 2019 Gordon Bell Prize Award Committee, during the International Conference for High Performance Computing, Networking, Storage and Analysis

(SC19) in Denver, Colo.

Today’s commercial microchips contain 100,000,000 transistors in the span of a single millimeter, and managing heat generation and dissipation is one of the central problems in computer architecture. As the transistors on each microchip have become smaller and more densely packed, the amount of heat they generate has steadily increased. The cooling systems needed to keep supercomputers and data centers from overheating have become increasingly expensive. The ETH Zurich researchers estimate that cooling can consume up to 40% of the total electricity needed for data centers, amounting to cumulative costs of many billions of dollars per year.

Today’s supercomputers, which can perform up to 200 quadrillion calculations per second, allow scientists in many disciplines to

for modeling nanoscale materials, but has experienced scaling bottlenecks. The ETH Zurich Team wrote a variation of OMEN that is Data Centric (DaCe OMEN). “We show that the key to eliminating the scaling bottleneck is in formulating a communication-avoiding algorithm,” the team writes in their paper. The ETH Zurich team’s solver yields data movement characteristics that can be used for performance and communication modeling, communication avoidance, and dataflow transformations. They go on to note that the speedup made by the DaCe OMEN framework is two orders of magnitude faster per atom than the original OMEN code.

The ETH Zurich team also built a graphical interface for the DaCe OMEN framework that includes a visualization of dataflow in lieu of a simple textual description. Anyone running the code can use the image representation to inter-



gain new insights by processing a staggering number of variables. The ETH Zurich team used their simulation to develop a map of where heat is produced in a single transistor, how it is generated, and how it is evacuated. It is hoped that a deeper understanding of these thermal characteristics could inform the development of new semiconductors with optimal heat-evacuating properties.

In recent years, the OMEN framework has been a popular quantum transport simulator

act with the data directly. The team believes this new innovation could be applied to numerous scientific disciplines beyond nanoelectronics.

Winning team members include Alexandros Nikolaos Ziogas, Tal Ben-Nun, Timo Schneider and Torsten Hoefler, from ETH Zurich’s Scalable Parallel Computing Laboratory, as well as Guillermo Indalecio Fernández and Mathieu Luisier from ETH Zurich’s Integrated Systems Laboratory.

The INSIDE TRACK

FROST & SULLIVAN

Rising Geopolitical Tensions Boost Military Spend on Electronic Warfare Equipment COTS releases

Evolving threat landscape, impending modernization of military aircraft to sustain demand for new, improved EW systems, finds Frost & Sullivan

The emergence of stealth and low observable aircraft along with Anti-Access/Area Denial (A2/AD) systems has made integrated air defense networks very complex and difficult to counter. Additionally, the development of new missile-seeker technologies for surface-to-air missiles poses a serious threat to aircraft as they bypass existing missile-detection systems. The presence of these new threats is driving the demand for modern electronic warfare (EW) systems that are sensitive enough to detect and engage targets before they are visually seen. A recent analysis of the global military airborne electronic warfare market forecasts the sector to rake in revenues over \$30.8 billion between 2018 and 2028, with \$21 billion worth of addressable opportunities arising from the planned and forecasted procurement of EW equipment.

"Many countries will be modernizing their aging fleets through upgrade or replacement programs in the next 10 years," said Ryan Pinto, Research Analyst, Aerospace and Defense at Frost & Sullivan. "With an increased focus on EW systems, this modernization phase will provide opportunities to replace their existing EW capabilities with modern systems that can counter new threat environments."

Frost & Sullivan's latest research, Global Military Airborne Electronic Warfare Market, Forecast to 2028, investigates the potential of military electronic warfare (EW) equipment in today's volatile geopolitical climate. The report explores the trends influencing electronic warfare and the factors driving sector growth, and offers a segment-wise analysis of the global electronic warfare market. The research also provides detailed revenue forecasts and identifies promising opportunities for growth in the sector.

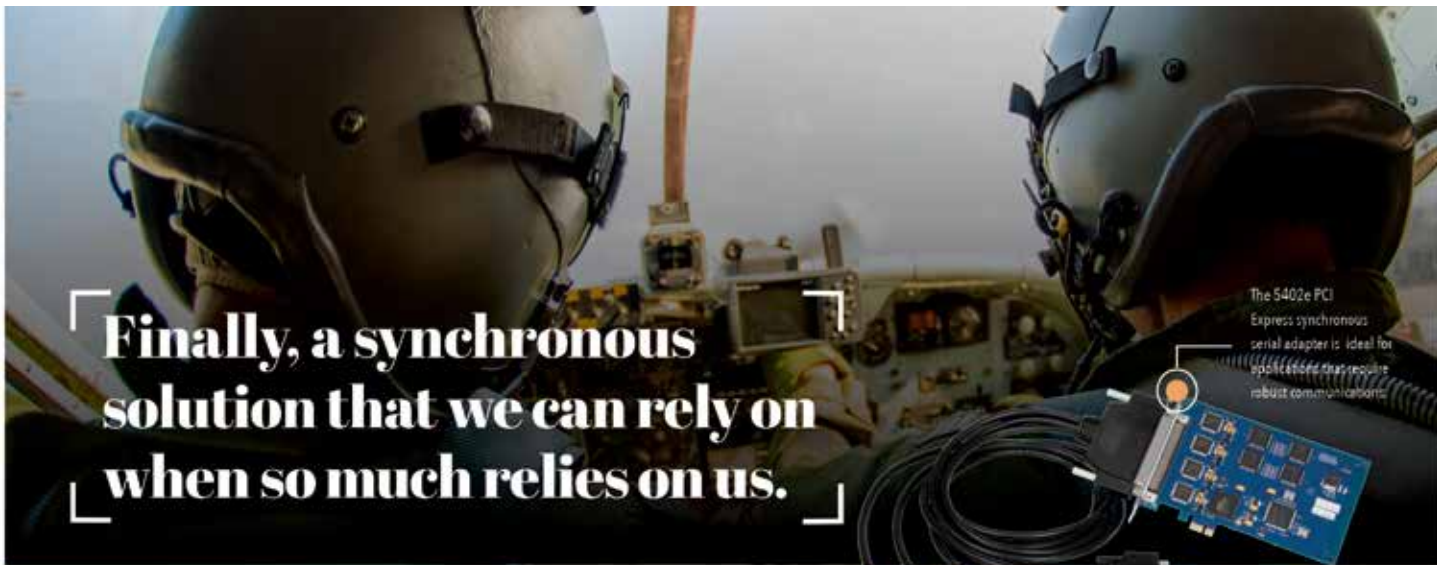
With Russia demonstrating its advanced electronic warfare capabilities in Ukraine and Syria, China has refocused its efforts toward showcasing similar capabilities in the Pacific. The two countries see EW as an important force

multiplier during a conflict. This has made bridging the EW capability gap a major priority for the US and NATO countries to maintain their advanced capabilities and remain competitive. New threats in the EW domain will drive new research and procurement programs.

"There is a growing need for indigenization and collaborative production, especially in emerging markets such as Saudi Arabia and India," noted Pinto. "Defense majors will have to vary their market strategy accordingly to access emerging opportunities in these markets."

Companies operating in this sector can also foster growth by:

- Offering more robust EW systems that would enable assets to conduct hybrid EW and CW tasks simultaneously.
- Developing faster signal processing and miniaturization to increase the sensitivity of jammers.
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- Reducing the size of EW payload to enable horizontal integration of multiple payloads.



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DCS Awarded \$93.4M Task Order to Support AFLCMC/WIH Helicopter Program Office

DCS Corporation has been awarded a 5-year, \$93.4 million prime task order to support the Air Force Life Cycle Management Center (AFLCMC) Intelligence Surveillance Reconnaissance & Special Operations Forces Directorate's Helicopter Program Office (HPO) under the Air Force's EPASS program. DCS will provide a broad range of acquisition, engineering, scientific, research, and administrative support for USAF aircraft research, development, production, life cycle acquisition, and sustainment.

Full performance will commence December 2019 from a new DCS facility near Wright-Patterson AFB, Ohio and will grow to include work at Duke Field (Eglin AFB Auxiliary Field #3) in Florida. Fully staffed, this effort is expected to comprise 95 personnel from DCS and subcontractors Naval Systems, Inc.; Sumaria, Inc.; and PE Systems.

"This is an exciting new opportunity for DCS to grow our Wright-Patterson AFB footprint and expand our support of DoD helicopters through these ACAT 1 programs," Executive Vice President Larry Egbert stated. "Our

rotary wing capabilities and background are well aligned to HPO mission requirements and we look forward to supporting the AFLCMC/WIH command and mission."



Ironwave Expands its RF and Microwave Capability for the Warfightere

Ironwave Technologies LLC announced its acquisition of American Microwave Corporation, based in Frederick Maryland. "The combined engineering and product offerings of our two American based companies allows us to expand into new markets", said Mr. Jim Guinaw, Executive VP of Sales for Mu-Del Electronics. "This acquisition will enhance our ability to support our Electronic Warfare and Communication Systems clients".

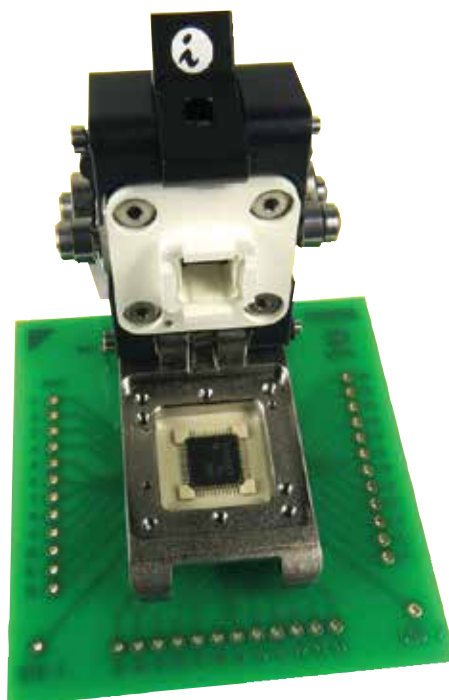
Mu-Del Electronics LLC, <https://www.mu-del.com>, based in Manassas Virginia, designs and manufactures radio frequency and microwave sub-systems and components for national defense purposes of intelligence collection, telemetry, radar signal processing and communication, in airborne, ground based and naval platforms

American Microwave Corporation, <https://americanmic.com>, is a leader in the design and manufacturing of DC to 40GHZ solid state control components and subsys-

tems for the communication and Electronic Warfare community since 1978.

Ironwave Technologies LLC invests in RF and Microwave technologies used in Elec-

tronic Warfare, communications, telemetry and surveillance. It has several current investments in the space and is actively pursuing additional acquisitions.



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The INSIDE TRACK

Sierra Technical Services Completes Major Milestone on 5GAT Drone for the Department of Defense

Sierra Technical Services, Inc. (STS) achieved a major milestone with the completion of Engine Run Testing on the 5th Generation Aerial Target (5GAT). The

5GAT contract is administered by the U.S. Army Corp of Engineers Contracting Office (US-ACE) located in Sacramento, CA and is man-



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aged by the Office of the Secretary of Defense, Director of Operational Test and Evaluation (OSD/DOT&E). STS was awarded a Prime Contract in March 2017 to design, manufacture, assemble, integrate and ground/flight test the 5GAT Demonstrator and has provided subject matter expertise to the U.S. Government while developing the design of the 5GAT aircraft concept since 2008.

The 5GAT aircraft is intended to meet specialized needs regarding "threat representative" adversaries that the U.S. Warfighter may encounter in an aerial combat situation. The 5GAT is a high-performance, unmanned, fighter-size aircraft that will be utilized for Air-to-Air and Surface-To-Air weapons evaluation, pilot training, and ground forces training when translated into production as the Next Generation Aerial Target (NGAT). The 5GAT Demonstrator First Flight is scheduled to take place early in 2020.

Roger Hayes, President and CEO of STS said: "This is an exciting day and major milestone achievement with the completion of these Engine Run Tests leading up to our flight test phase expected in the 1st quarter of 2020. I am extremely proud of our very small and dedicated 5GAT Team. This is a major step forward to providing our warfighters an attritable, low-cost, high-performance, full-scale, 5th Generation Aerial Target that can be also be used by the Department of Defense (DoD) for other emerging projects such as NGAT, Loyal Wingman, and Sky Borg."

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Rugged RF & Optical Solutions Over OpenVPX Prepare Mil/Aero Customers For the Next Generation of System Performance

By Justin Moll, Vice President, Sales & Marketing, Pixus Technologies

Military and Aerospace embedded computing systems are evolving quickly and the industry is striving to meet the changing requirements. One area of significant advancement is the OpenVPX backplane arena, with a strong push from the Army's CERDEC with the CMOSS (C4ISR/EW Modular Open Suite of Standards) effort, Navy's NAVAIR with HOST (Hardware Open System Technologies), and Air Forces' AFLCMC with FACE (Future Airborne Capability Environment) and SOSA (Sensor Open Standard Architecture) to move jointly toward an open, compatible architecture. Okay, enough acronyms. In short, the industry is adding more power and bandwidth/performance to OpenVPX-based systems.

More bandwidth, performance

There is a broad range of backplane speed requirements for tomorrow's advanced systems. Many applications will work just fine for years to come with 10GbE and PCIe Gen2 speeds across the slots of the system. But, others have requirements where speed is paramount. The approximately 12.5 Gbps limitation of the current MultiGig RT2 OpenVPX connector won't cut it for 100GbE (4 lanes x 25 GbE) or even PCIe Gen4 (16 Gbps). The good news is the new RT3 version of the connector is backwards compatible (from a Plug-In Module perspective) and is designed to 25 Gbps speeds.

It isn't only the speed across the OpenVPX backplane connectors that is increasing. VITA 66 adds various optical connector options and VITA 67 adds RF connector options.

This allows a blind-mate optical and/or RF interface to be used on OpenVPX modules. There are all types of requirements and configurations with these subsets. This requires a lot more configuration for backplanes. To help alleviate this challenge, development backplanes have been developed for some of the configurations. See Figure 1 Those seeking to prepare for SOSA/HOST or other requirements are utilizing various combinations of these interfaces. While SOSA calls out for aggressive implementations for advanced cooling, including airflow going directly through the pluggable modules, it seems likely that a wide range of thermal management options will be utilized. We can take a lesson from the AdvancedTCA architecture from the early 2000's. The specification required full redundancy throughout the shelf

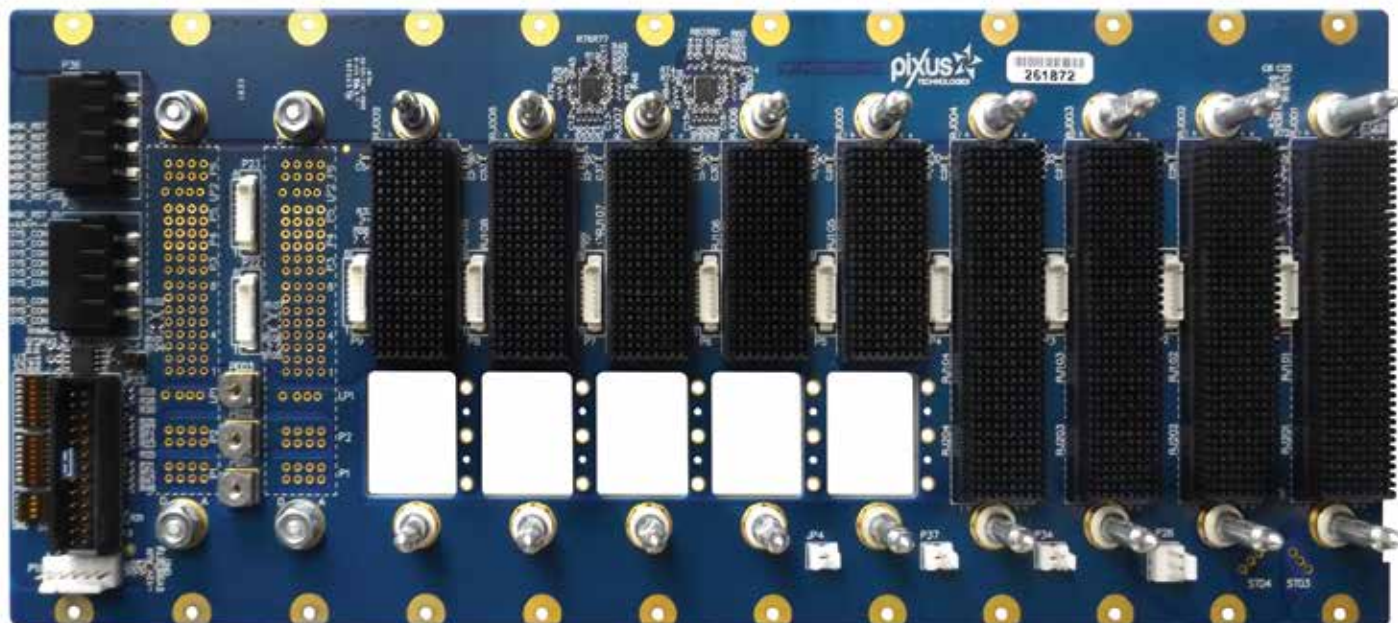


Figure 1 - A wide variety of development and deployable backplane for OpenVPX support new VITA 66/VITA 67 boards. This 9-slot example has four slots with cutouts to install VITA 66.4 optical connectors.

(chassis platform). However, as the market evolved implementations emerged with a single shelf manager, AC (single and dual) power supplies, etc. The cooling configurations evolved from front to rear to side-to-side airflow and even some conduction-cooled versions. It seems likely that the rugged MIL OpenVPX market will evolve to “what works” regarding the cooling implementations. In some cases, the more powerful standard cooling approaches can be highly leveraged (see more on this below). The new VITA specifications where the airflow is channeled on the outside of the module looks to become an easy middle ground. The change to current chassis designs is minimal to direct air through these channels on the outside of the module. The more complex route is an air-flow-through-module approach, where the air would be channeled into a module canister. This would require more significant changes to the cooling approach for an air-cooled system, but the principle is similar to that of an ARINC600 enclosure, where an external air source channels the air in a duct to enhance the cooling of the sealed unit.



Figure 2 - The SOSA/HOST effects are beginning to employ VITA 46.11 Chassis Managers for OpenVPX. This example board can plug into any standard OpenVPX slot via the P0 connector.

VITA 46.11 System Management

Utilizing the system management feature of VITA 46.11 is another target of these types of applications. The chassis manager main-

ly monitors the power and system thermals. For example, it can monitor each of the power rails and provide an alarm function for voltage levels that fall below the defined



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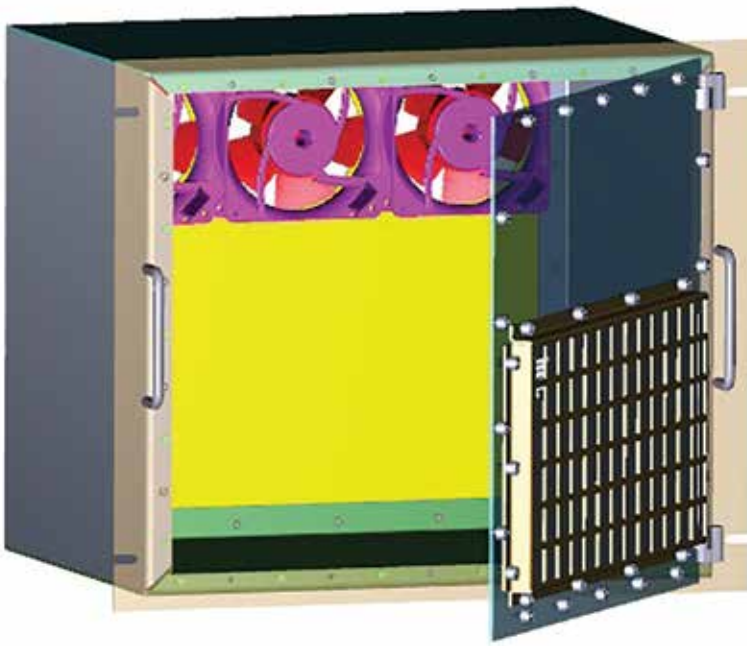


Figure 3 - Rugged rackmount OpenVPX chassis leverage powerful cooling to dissipate the higher wattages of new modules. This model example pulls air through the card cage in a front-to-rear cooling configuration.

acceptable range. An OpenVPX chassis manager can be used to monitor cooling zones with thermal sensors located in the chassis. The fan control function can automatically speed up as needed to cool each zone properly. Figure 2 on previous page shows an example of an OpenVPX Chassis Manager. This design plugs into the P0 (power and system management) connector of any OpenVPX backplane. Various front panels can be utilized to fit the needs of the system

such as 3U or 6U and 4HP (0.8") wide or 5HP (1.0") wide. Additionally, a version in wedge locks for conduction cooling is also possible. For more I/O and customization, a P1 and/or P2 connector can be added.

Rugged Chassis Designs

To meet the MIL specifications, the chassis needs to have a few key elements. First, the enclosure must be ruggedized with thicker rails, metal sidewalls, etc, to handle the shaking of the system. With requirements to operate in often -40 to +70C or even higher temperature levels, MIL-grade fans need to be employed. The chassis manufacturer can do thermal simulation to approximate the CFM and cooling options to meet each application's needs. The subrack is typically recessed inside the chassis with an EMI protective door that allows enough air intake while restricting emissions. In most cases, an AC or DC VITA 62 compliant PSU will be utilized. These power supplies are compliant to the MIL specifications and some have special options for airborne requirements. See Figure 3 for a model of an 8U MIL rugged OpenVPX chassis. The chassis is de-





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signed to accept up to 15 OpenVPX slots and 1 pluggable VITA 62 PSU slot or various configuration options therein. A similar approach can be employed for 3U modules in a 5U high MIL chassis. With three high CFM MIL grade fans, the chassis can dissipate a significant amount

tional cooling. While this type of chassis is used in many defense and industrial server room type of applications, it can also be utilized as a development and demonstration platform. Some engineers have chosen to implement this cooling approach in a version

maintenance, etc, the system designers still want conformal coating and some EMI and environmental/temperature protections.

The semi-rugged enclosures are common in the horizontal-mount approach. These



Figure 4 - Horizontal-mount OpenVPX chassis platforms can save significant rack space. The 2U high chassis in this example pulls air in a front-to-rear airflow configuration, but can be modified for side-to-side cooling requirements.

of heat. The I/O cabling is an important issue in order to ensure there is ample space for the I/O and that it doesn't impede the airflow substantially.

Other Chassis Design Types

While most OpenVPX applications require some degree of MIL grade shock/vibration, EMI, and environmental protection, there are also benign environment designs that provide powerful cooling. One example is a 16-slot OpenVPX chassis with dual blowers that pull air from an intake area below the subrack and blow the heat 90 degrees out the rear. This approach allows the use of full Rear Transition Modules (RTMs) plugging into the rear of the backplane. The dual 191 CFM fans can cool up to 2000W (125W/slot in a full 16-slot chassis with a 1" pitch) in a 9U high chassis for 6U OpenVPX boards or a 7U high chassis for 3U OpenVPX boards. A 10U version allows more air intake for addi-

with thicker metal and other light-rugged requirements. The fans can be latched to meet lower to moderate levels of shock/vibration. When it's time to go to a deployed unit, the other aspects of the system (types of fans, recessed subrack, etc) can be implemented. There are also applications where there is a lighter range of shock/vibration such as 10-15G of shock and 2.5G-4G at 1-50Hz of vibration at standard test intervals of time. These semi-rugged designs can be utilized in various sizes and types.

Semi-Rugged Design Types

Many applications do not require the heavy 25G+ level of shock requirements. But, the standard industrial-grade chassis design isn't enough. Semi-rugged designs are an excellent middle ground, where they will provide a high degree of reliability and certainty placed within a MIL grade cabinet. Although the chassis is protected inside the cabinet, for

chassis platforms save rack space by loading the boards horizontally in the 19" rackmount system. When the slot count is low (usually 6 OpenVPX slots or less at 1" pitch), this approach can be an important space-saver. This is especially true when just a couple of slots are required. Figure 4 shows a 2U tall horizontal-mount 19" chassis example that supports two 6U OpenVPX boards or four 3U OpenVPX boards or a hybrid mix.

More Performance

As applications move to the advanced cooling plans of SOSA/HOST and the related initiatives, we will likely see a broad mix of chassis platform configurations in the meantime. This includes non-rugged, semi-rugged, and MIL rugged approaches. Regardless of the chassis type, the backplane speed – along with optical and RF connection options keep ramping up to new performance levels.

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Leidos

By John Reardon, Editor

Leidos has a legacy of important work in national security, healthcare, engineering and infrastructure. At the age of 45, with a wife and three kids, J. Robert Beyster, Ph.D., officially launched his new company under the name Science Application Incorporated. The US government becomes the company's first customer, hiring the company to analyze the effects of nuclear weapons. A surprise to Dr. Beyster the company made a profit in its first year of operations.

As the company moved into a new decade the company won a contract studying radiation-based cancer therapy for the Los Alamos National Laboratory. This was the beginning of the company's health care business. In 1972 an office was opened in Albuquerque in support of the Air Force Weapons Laboratory. The company assists the lab with their work on electromagnetic phe-

nomena and effects. This became the Physical Science Group.

As the company grew in prominence, it won a large contract with the Kuwaiti Defense Forces. The decade closed out with a contract to assist in the clean up of Three Mile Island Nuclear station in Pennsylvania. The site of the worse nuclear disaster in the US history, the company played a vital role in the clean up.

In 1987 the company was recognized around the world for their contribution to the design of Star and Stripes, the America's Cup Boat sailed by Dennis Conner. The approach and success that the company was able to achieve proved to the world that the engineering talents and the methods employed were world class. Stars and Strips returned the America's Cup back to the United States.





Image 1 - Leidos to provide U.S. Army Common Driver Training systems services

As the company grew it was able to pursue larger and larger contracts and in 1988 the company won its first billion-dollar contract to create the Department of Defense's (DoD) Composite Health Care System and to deploy it to more the 500 medical facilities worldwide.

The company, known for its employee ownership, was taken public by the CEO of the time, Kenneth Dahlberg. Going public on the New York Exchange, the company saw a post IPO increase of 21%.

The company continued with its knowledge and understanding

*Leidos employs over
34,000 individuals in
400 locations around
the world.*





Image 2 - Metropolitan Police appoints Leidos UK to upgrade Command and Control system responsible for officer deployment

of how to deal with clean up at nuclear power sites with a \$3 billion contract at the Hanford site. This prompted the company to move its corporate head quarters to McLean, Virginia. In 2011 the company won a \$2 billion contract with the National Science Foundation to provide support and maintenance for the U.S. Antarctic Program.

In September of 2013 the company split into two companies – Leidos and SAIC. Leidos was a \$7 billion solutions provider and the new SAIC was a service provider. In early 2019 the Leidos merged with the IT solutions group of Lockheed Martin. This created a monster of a company with over \$10 Billion dollars in revenue. The Lockheed shareholders retained 50.5% of Leidos. The company has three divisions: Biomedical Research, Digital Solutions and Health. The impact of Leidos is broad and varied with advance in cancer research and civil aviation.

The company employs over 34,000 individuals in 400 locations around the world.



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January 2020 COT'S PICKS

Pentek Announces 6.4 GHz A/D and D/A Jade 3U VPX Module for Wideband Defense, Radar and Communication Applications

- Utilizes state-of-art high-speed Texas Instruments A/Ds and D/As
- Matching 6.4 GHz A/D and D/A sampling for wideband signals
- 3U VPX with PCIe Gen.3x8, Optical I/O and RF I/O backplane options
- Jade architecture uses Xilinx Kintex UltraScale FPGA
- Navigator Design Suite supports Xilinx Graphical Vivado IP Integrator

Pentek, Inc., introduced the newest member of the Jade™ family of high-performance data converter 3U VPX modules based on the Xilinx Kintex Ultrascale FPGA. The Model 54141A is a dual channel analog-to-digital and digital-to-analog converter with sample rates up to 6.4 GHz. Programmable DDCs (digital downconverters) and DUCs (digital upconverters) support connections to IF or RF signals.

"The 54141A combines our popular 7114A XMC module with a 3U VPX carrier, yielding a powerful, forward-looking package for very wideband communications or radar applications that require advanced I/O resources," said Rodger Hosking, vice-president of Pentek, Inc.

Not only does the Model 54141A comply with the VITA 65.0 3U VPX specification, it also offers flexible analog and digital interface options for the VPX P2 backplane connector to meet system-specific requirements. In addition to its PCIe Gen.3x8 interface on the VPX P1 connector, it is possible to add up to 8 more gigabit serial lanes connected directly to the FPGA for supporting user-installed protocols.

The Model 54141A supports the emerging VITA 66.5 optical interconnect standard by providing four optical duplex lanes to a mating spring-loaded backplane connector. With the installation of a serial protocol like 10 or 40 Gigabit Ethernet in the FPGA, the interface enables high-bandwidth digital communications between boards or chassis independent of the PCIe interface.

For flexibility across different I/O requirements, the board can be optioned to support VITA 67.3C. This provides analog signal routing through the VPX backplane to replace front panel connectors for RF

In/Out, Sample/Reference clocks and Gate/Trigger/Sync/PPS signals. This option is often required in ruggedized deployments and for simplifying unit field replacements and upgrades.

A/D Stage and Digital Down-converter

The Model 54141A uses the Texas Instruments ADC12DJ3200 12-bit A/D converter with an input bandwidth of 6 GHz, which operates in single-channel interleaved mode with a sampling rate of 6.4 GHz or in dual-channel mode with a sampling rate of 3.2 GHz.

Digital Up-converter and D/A Stage

A Texas Instruments DAC38RF82 D/A with DUC accepts a baseband real or complex data stream from the FPGA and delivers it to the interpolation, up-conversion and dual D/A stages for output signals up to 4 GHz. The two 6.4 GHz 14-bit D/As pair well with the dual input channels while delivering more than twice the output performance of previous generations of Pentek products.

Performance IP Cores

The Model 54141A factory-installed functions include two A/D acquisition modules and a D/A waveform generation IP module. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe Gen.3x8 interface complete the factory-installed functions. An optional VITA 49.2 data transport protocol IP module conveys digitized signal metadata for signal acquisition and processing elements in communication, radar or storage systems. System integrators get to market with less time and risk, because the Model 54141A can provide a complete turnkey acquisition/generation solution, often without the need to develop FPGA IP.

The Jade Architecture

The Pentek Jade Architecture is based on the Xilinx Kintex UltraScale FPGA, which raises the digital signal processing (DSP) performance by over 50% with equally impressive reductions in cost, power dissipation and weight. As the central feature of the Jade Architecture, the FPGA has access to all data and control paths, enabling factory-installed functions

including data multiplexing, channel selection, data packing, gating, triggering and memory control. A 5 GB bank of DDR4 SDRAM is available to the FPGA for custom applications. The x8 PCIe Gen 3 link can sustain 6.4 GHz data transfers to system memory. Eight additional gigabit serial lanes and LVDS general purpose I/O lines are available for custom solutions.

Navigator Design Suite for Streamlined IP Development

Pentek's Navigator™ Design Suite consists of two components: Navigator FDK (FPGA Design Kit) for integrating custom IP into Pentek sourced designs and Navigator BSP (Board Support Package) for creating host applications. Users can work efficiently at the API level for software development and with an intuitive graphical interface for IP design. The tools reduce the development time and cost associated with complex designs. The Navigator BSP is available for Windows and Linux operating systems. Unlike others in the industry, Pentek still provides application support to customers at no cost.

*Pentek Inc.
www.pentek.com*



January 2020 COT'S PICKS

New Rugged Supercomputing Servers Enable AI, HPC and Sensor Fusion Applications at The Edge

Latest field-deployable parallel computing subsystems optimize big data workloads for mission-critical platforms

Mercury Systems, Inc. unveiled the EnterpriseSeries™ RES AI rugged rackmount server line, bringing High Performance Computing (HPC) capabilities to aerospace, defense and other mission-critical applications at the edge.

“The proliferation of sensors, ever-growing data loads and the evolution of complex deep learning neural networks continues to increase computational demands, driving the need for supercomputing infrastructure closer to the edge,” said Scott Orton, Vice President and General Manager of Mercury’s Trusted Mission Solutions group. “Through close collaboration with technology leaders such as NVIDIA and Intel, we’ve developed reliable parallel computing systems that accelerate demanding artificial intelligence (AI), signal intelligence (SIGINT), and sensor fusion applications where it’s needed the most.”

Why it Matters: Evolving compute-intensive AI, virtualization, big data analytics, SIGINT, autonomous vehicle, Electronic Warfare (EW) and

sensor fusion applications require data center supercomputing capabilities closer to the source of data origin. Delivering HPC capabilities to the edge presents challenges as every application has its own security, performance, footprint, budget and reliability requirements. To address this need, Mercury partners with technology leaders to align technology roadmaps and deliver cutting-edge computing in scalable, field-deployable form-factors that are fully configurable to each unique workload.

What it delivers: Mercury’s rugged HPC servers leverage the latest data center processing and co-processing technologies to accelerate the most demanding workloads. Customer benefits include:

- The ability to scale supercomputing applications from the cloud to the edge with rugged subsystems that adhere to open standards and integrate the latest commercial technologies.
- Maximized throughput through contemporary NVIDIA® graphics processing units (GPUs), Intel® server-class processors, field-programmable gate array (FPGA) accelerators, and high-speed networking.
- Optimized performance for almost any mission-critical platform with multiple form-factors that withstand a broad range of field environments
- Advanced security options that deliver trusted performance and safeguard critical data
- Extended system longevity and product life-

cycles to support the needs of aerospace, defense and other mission critical operations.

Scalable Computing:

Engineered to handle massive workloads anywhere, Mercury’s supercomputing servers integrate the latest NVIDIA® GPUs and Intel® Xeon® Scalable processors in environmentally resilient, rugged, expandable form-factors. To optimize performance in a small footprint, RES AI servers densely pack multiple processors and expansion slots in a range of compact chassis to support the unique application and deployment requirements of customers.

Maximized Throughput:

Powered by NVIDIA Volta, Pascal™ and Turing™ architecture GPUs, Mercury’s subsystems harness parallel processing to maximize throughput, boost productivity and push the boundaries of compute-intensive applications. A single RES AI 4U server supports up to eight NVIDIA V100 Tensor Core GPUs.

Optimized performance in extreme conditions:

Built from the ground up to provide edge computing capability previously reserved for the datacenter, field-deployable RES AI servers incorporate innovative patented technologies and design features to withstand shock, vibration, dust, sand, and temperature extremes. To ensure uptime, availability, and sustained optimal performance in almost any environment, RES AI servers are certified to multiple military (MIL-STD) and commercial (IEC) environmental specifications.

Trusted and Secure:

For security-imperative applications, Mercury’s servers can be customized with U.S. designed and manufactured motherboards and unique hardware and software protection layers that safeguard critical IP. When configured with Mercury’s self-encrypting, defense-grade solid state drives (SSD), RES AI delivers data-at-rest protection. A multi-platform compatible, secure hypervisor option that guards against cyberattacks, is also available.

*Mercury Systems, Inc.
www.mrcy.com*



January 2020 COT'S PICKS

Abaco Announces Industry's First 6U VPX Solution to Feature new Xilinx RF System-on-Chip Technology

Abaco Systems announced the industry's first 6U VPX implementation of the transformational Xilinx® 16x16 RF system-on-chip (RFSoc) technology combined with the Xilinx Ultrascale+™ FPGA with High Bandwidth Memory (HBM). The VP460 Direct RF Processing System is aligned with the SOSA™ standard to deliver the cost-effective interoperability required by the US Air Force, Army, and Navy.

The new 6U VPX platform complements the previously announced VP430 3U VPX Direct RF Processing System.

Designed to enable development of advanced, next generation multi-channel electronic warfare systems in application areas such as MIMO, beamforming, sensor processing, radar, SDR and signals intelligence, the VP460 is

characterized by its very high performance and channel density. It features 16 integrated analog-to-digital converters at 2GSPS, and 16 digital-to-analog converters at 6.4 GSPS. Also included are a user-programmable FPGA fabric and multi-core Zynq® ARM® processing subsystem. The HBM VU37P device features the speed and capabilities of an UltraScale+ FPGA together with integrated DRAM in the FPGA package, and is capable of up to 460GB/s on-chip data transfer rates.

By reducing RF signal chain complexity and leveraging heterogeneous processing capabilities, the VP460 allows input/output channel density to be maximized and data offloaded more efficiently - without sacrificing onboard signal processing capabilities.

"Today's electronic battlefield is seeing the accelerated growth of smart sensor systems - and is demanding more channels, more bandwidth, and as a result, more data processing capabilities," said Peter Thompson, Vice President, Product

Management at Abaco. "The VP460 is a revolution in COTS RF and FPGA processing, perfectly balancing the need for high performance FPGA processing, the ease of a hardened embedded processor and the ultra-low latency of integrated analog interfaces."

"With its ability to synchronize all 16 channels, as well as multiple boards for even larger system applications, the VP460 is one of the densest 6U VPX analog FPGA carrier boards available," Thompson continued. "In previous generations of technology, this combination would have taken four times as many boards. It can make a significant contribution to minimizing SWaP - which is vital in the increasingly constrained environments in which today's systems are being deployed."

With 16 ADCs sampling at rates up to 2GSPS with two bytes per sample, even the modern PCIe™ Gen3 high-speed data connection is too slow for a direct transfer. To overcome this challenge, the VP460 includes - in addition to the PCIe Gen3 data plane - up to 64 high speed serial lanes to the Xilinx Virtex™ Ultrascale+ HBM device, supporting protocols such as PCIe Gen3, 10/40G Ethernet, Aurora and so on.

The new Xilinx RFSoc is a revolutionary step in integration technology bringing a combination of Field Programmable Gate Array (FPGA) processing capability, a multi-processor embedded ARM® Cortex-A53 Application processing unit (APU), and an ARM real time processing unit (RPU). Additionally, the Zynq® Ultrascale+™ architecture integrates all this with features to enable high security IP protection.

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January 2020 COT'S PICKS

MoSys Announces New Software Targeting Packet Classification Applications

Announcing Graph Memory Engine™ Running on Xilinx UltraScale+ with TCAM Compiler

The Packet Classification Platform will make use of MoSys' innovative virtual accelerator, the Graph Memory Engine (GME), for performing embedded search and classification of packet headers as an alternative to TCAM functions. The platform includes the GME and software that compiles TCAM images into graphs for GME processing using a common API for

PHE version provides enough performance to support two 100G ethernet ports.

"Along with making acceleration available to a wider set of environments, MoSys enables the software designer to make use of hardware performance without developing firmware or RTL," noted Michael Miller, MoSys' chief technical officer. "Moreover, similar to the GME, the same approach can be applied to a wide variety of advanced embedded applications including key value pair databases, networking search functions, machine learning, computation and algorithm acceleration, all of which can run on different hardware platforms."

New platforms will be rolled out over the next few quarters to address other markets. Target applications include acceleration cards, 5G edge compute, aerospace and defense, advanced video, high-performance computing and other data-driven applications.

"We are delighted to see MoSys expanding its product strategy in this direction," noted Farhad Shafai, vice president, communications markets, Xilinx. "Our industry-leading FPGAs already have proven experience interfacing with MoSys' Bandwidth Engine serial-memory devices to accelerate networking and security applications. We look forward to collaborating with MoSys on its new platform to enable customers even higher, more scalable performance and flexibility using our advanced adaptable solutions."

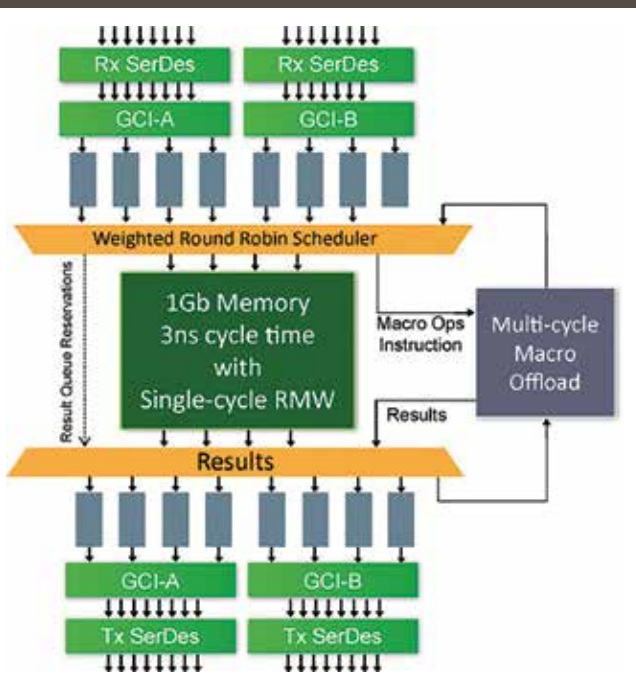
MoSys is currently in discussions with early access customers and expects to formally release the products in the first quarter of 2020.

At the recent series of Xilinx Developer Forums, MoSys successfully demonstrated its packet classification and layer 2 forwarding capability targeted at FPGA-based SmartNIC, router, switching, security and cloud applications. The interactive demonstration featured a TCAM compiler, classifier and a Layer 2 forwarding database running on a MoSys PHE connected to a Xilinx VU9P UltraScale+ FPGA on a PCIe card plugged into a standard server box.

MoSys
mosys.com

portability. The GME is provided as a family of implementations ranging from a pure software version for maximum flexibility and capacity, RTL for use in a Xilinx FPGA for hardware performance, and a maximum performance RTL solution connected to a MoSys Programmable HyperSpeed Engine (PHE) with its 32 embedded RISC cores. The initial FPGA versions of the GME are compatible with Xilinx UltraScale+ and utilize a common RTL interface to facilitate platform portability.

The search performance on an UltraScale+ FPGA with MoSys PHE can result in up to 100x performance over software solutions running on host CPUs with DRAM, which are bottlenecked by random accesses of memory. The



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January 2020 COT'S PICKS

Microchip's Low-Power Radiation-Tolerant (RT) PolarFire® FPGA Enables High-Bandwidth Space Systems with Lower Total System Cost

Industry's lowest-power FPGA enables high-throughput on-orbit processing systems that withstand radiation effects in space

Developers of spacecraft electronics use radiation-tolerant (RT) field programmable gate arrays (FPGAs) to create on-board systems that meet the demanding performance needs of future space missions, survive the brutal launch process and continue to operate reliably in the harsh environment of space. Extending its RT FPGA offering to bring these capabilities to emerging high-performance space applications, Microchip Technology Inc. (Nasdaq: MCHP) today introduced the RT PolarFire FPGA that is optimized to meet the most demanding requirements in spacecraft payload systems' high-speed data paths with the lowest possible power consumption and heat generation.

"We are supporting an evolving set of on-orbit space applications that need high levels of operating performance and density,

low power consumption and minimal heat dissipation, while reducing system-level costs," said Bruce Weyer, vice president of Microchip's FPGA business unit. "Our RT PolarFire FPGA enables the major leap in computing throughput required for these applications including processing-intensive neural networks for object detection and recognition, high-resolution passive and active imaging, and high-precision remote scientific measurement, while maintaining a path to QML qualification."

A growing number of space applications need greater computational performance so they can transmit processed information rather than raw data and make optimal use of limited downlink bandwidth. The RT PolarFire FPGA enables this at significantly lower cost and with faster design cycles than possible with application-specific integrated circuits (ASICs). It also significantly reduces power as compared to the alternative of using FPGAs based on static random access memory (SRAM) while eliminating their vulnerability to radiation-induced configuration upsets. The RT PolarFire FPGA is supported by all necessary radiation data, specifications, package details and tools customers need to start new designs now, initially with the commercial version of the device.

The RT PolarFire FPGA builds on the success of Microchip's RTG4 FPGA, which has been widely deployed in space applications that require its radiation-hardening by design against single event upsets (SEUs) and inherent immunity to single event latch-ups (SELs) and configuration upsets. For space applications that require up to five times the computing throughput, the RT PolarFire FPGA provides 50 percent more performance and triple the logic elements and serializer-deserializer (SERDES) bandwidth. It also provides six times the amount of embedded SRAM to enable more system complexity than previously possible using FPGAs and withstands total ionizing dose (TID) exposure beyond the 100 kilorads (kRads) that is typical of most earth-orbiting satellites and many deep-space missions.

The RT PolarFire FPGA cuts power consumption to approximately half that of alternative SRAM-based FPGAs with equivalent density and performance. Its SONOS non-volatile (NV) technology enables its configuration switches to be implemented in a more power-efficient architecture that cuts development and bill of materials costs through simplified, less expensive and lighter power system design while minimizing heat dissipation to reduce thermal management problems. Designs are further simplified as compared to using SRAM-based FPGAs because the RT PolarFire FPGA eliminates the cost, complexity and recovery downtime of mitigating configuration SEUs.

The RT PolarFire FPGA will undergo the standard process for meeting QML standards including class V qualification for highly critical applications. Microchip has lengthy experience achieving QML qualification for its RTG4 FPGAs and other products, which requires extensive and continuous testing including screening each wafer and package assembly lot.

Microchip
www.microchip.com



January 2020 COT'S PICKS

MoSys Announces Function Accelerator Platforms Scalable Over Diverse Hardware Environments Expands Business Model to Include New Software Accelerator Product Line

MoSys, Inc. announced a strategic new direction with the introduction of its Software Accelerator Product Line. The new product line includes a family of Function Accelerator Platforms, which target specific application functions and use a MoSys common software interface to allow performance scalability over multiple hardware environments.

This software-defined, hardware-accelerated platform architecture enables system designers to reuse internally developed software code using MoSys' common software interface across multiple hardware environments depending on the performance required. MoSys' new application-targeted Function Accelerator Platforms are hardware agnostic and operate with or without a MoSys IC. The platforms can run on a CPU or FPGA that is not attached to a MoSys IC or an FPGA that is attached to a member of the MoSys Accelerator IC family, including the Bandwidth Engine or Programmable HyperSpeed Engine with inmemory compute capability. Using one of these new platforms, MoSys expects that acceleration, scaling from a CPU only to a FPGA attached to a MoSys IC, can be as high as 100 times.

The Company believes that these new MoSys scalable solutions will meet today's applications needs, as well as provide a path to new products with flexibility to address new, more performance-driven market demands. New hardware system platform designs will need to scale to higher performance, and MoSys expects the Function Accelerator Platforms to increase new application demand for its current Accelerator IC products. As networking and other applications continue to migrate to software-defined environments, most notably software-defined networks (SDN), performance scaling has become key to remaining competitive while addressing the growing requirements being placed on the network.

Software now must be transferrable across

multiple hardware environments in order to be both cost-effective and provide the required flexibility to meet changing performance demands. "We anticipate that our new software and IP product licensing strategy will allow us to bring to market products that expand our current business model beyond silicon ICs," noted Dan Lewis, President and CEO of MoSys. "We believe these new software-focused platforms can contribute to growth in multiple ways. First, they may allow MoSys to expand with higher gross margin products in its currently served available markets by providing higher-value solutions, and, second, of more importance, offer products to previously unaddressed, new markets." Each Function Accelerator Platform will be comprised of a MoSys Virtual Accelerator Engine (VAE), which represents a range of software and firmware implementations

of the same accelerator function (e.g., search, classification, etc.), employing a common application program interface (API), and, with FPGA versions, a common RTL interface, to allow platform solutions to easily achieve performance scaling. In addition, some function platforms will include support tools to facilitate both software and hardware design. "With these new software-defined, hardware-accelerated

solution platforms, MoSys intends to push the boundaries of what a network can achieve," noted Michael Miller, MoSys' CTO. "We are developing embeddable function platforms for accelerating search, storage, classification, security, AI and other data-analysis applications that will provide a simple migration path for our customers with a straight-forward performance scalability path." A key benefit of each VAE lies in the use of a common API.

Once performance requirements are identified, the appropriate hardware platform can be selected. For the system engineer, this means platform portability and the opportunity for a wider range of products in a shorter period of time. Because the workload configuration and management will all be accomplished through a high-level language API, the burden on software application engineers to understand RTL or do firmware coding is minimized.

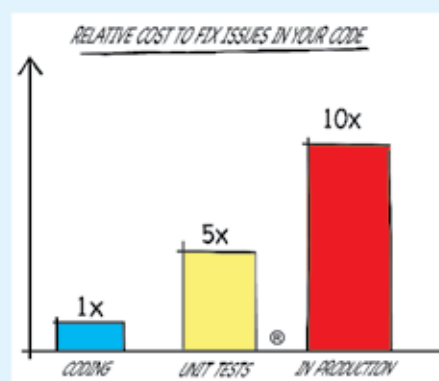
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January 2020 COT'S PICKS

WIN Enterprises Announces 2U HPC Hybrid Cloud Server with Dual Intel® Xeon Processors for IoT, Call Center and the Cloud

WIN Enterprises, Inc. announces the PL-82010, a hybrid cloud computer with dual, high-performance, Intel® Xeon Scalable processors. The server supports two scalable 64-bit Intel® Xeon processors for use in Cloud, IoT, and Call Center applications. Hybrid cloud computers provide the flexibility to handle private, proprietary data while allowing utilization of third-party cloud services for less-critical data. Robust I/O capabilities provide application flexibility, easy manageability, power efficiency, and faster data throughput.

FEATURES

- Dual Intel® Xeon® Scalable Processor Platforms
- 2U/12 Bays TPCS System
- 12x DDR4 ECC-RDIMM/LRDIMM/3DS LRDIMM 2400, 2666
- (4+2) 1G BaseT LAN ports / 4x 10GbE SFP+
- 80+ Platinum Certified 550W/850W CRPS
- Supports WIN Trusted Platform Control Module

High-speed data analysis is supported by 24 processing cores per Intel® Xeon CPU. Data originated at edge-deployed IoT devices is sent to a PL-82010 central network server for analysis. The server, a key part of this IoT infrastructure, is typically located in the data center. The data is processed and instructions sent back to the edge-deployed devices. Critical information is protected during these transactions through support of a TPC Module (TPCM). The PL-82010 provides 3TB of DDR4 memory. I/O includes 4x 10GbE SFP+, plus robust PCIe expansion slots that can provide additional LAN support.

Data transfer is augmented with 2x M.2 NVMe 2280. The M.2 feature accelerates the transfer of data between the enterprise call center, client systems and solid-state drives (SSDs) using a high-speed Peripheral Component Interconnect Express (PCIe) bus. High-speed networking is important here, as latency can negatively impact the functioning of the production line-based monitoring devices.

In addition, PL-82010's can be deployed in the cloud by service providers to build a high performance computing (HPC) cluster. Storage is provided by 12x 3.5" hot-swap SATA/SAS SSDs; 4x 3.5" hot-swap SATA/SAS SSDs, and 2x M.2 NVMe chips per unit.

The PL-82010 platform can be modified based on a customer's unique market requirements.

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